IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	
ELIYAHOU HARARI, ROBERT D. NORMAN and SANJAY MEHROTRA	Group Art Unit: 2785
Serial No.: 08/931,133	Examiner: P. Chung
Filed: September 18, 1997	
For: FLASH EEPROM SYSTEM	San Francisco, California

Assistant Commissioner of Patents
Washington, D.C. 20231

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231 on May 28, 1998.

Brenda J. Dolly
Brenda J. Dolly May 28, 1998
Signature Date

REQUEST FOR SUPPLEMENTARY OFFICE ACTION

Sir:

A first, non-final Office Action, dated May 20, 1998, was received in the above-identified patent application. However, additional claims 68-72, added by a Second Preliminary Amendment, filed on February 17, 1998 (according to a stamp on the returned postcard receipt) were not considered. Nor is there any indication in the Office Action that the three binders of references submitted with an Information Disclosure Statement file on that same day have been considered.

Therefore, it is respectfully requested that the Office Action be supplemented to act on the new claims and make the references cited in the Information Disclosure Statement of record. A copy of the February 17, 1998 filing is enclosed, including the return postcard receipt but without the three binders containing copies of the cited references.

Dated: May 28, 1998

Respectfully submitted,

Gerald P. Parsons, Reg. No. 24,486
MAJESTIC, PARSONS, SIEBERT & HSUE P.C.
Four Embarcadero Center, Suite 1100
San Francisco, California 94111-4106
Telephone: (415) 248-5500
Facsimile: (415) 362-5418

Atty. Docket: HARI.006USG

Serial No. 08/931,133 Atty. File No. HARI.006USG By GPP:bjd

In the Matter of the Application of Eliyahou Harari et al

Flash EEPROM System

The following has been received in the U.S. Patent & Trademark Office on the date stamped hereon:

____	Patent Application Specification	____	Notice of Appeal
____	Express Mail	____	Extension of Time Request
____	Power of Attorney/Declaration	✓	~~Amendment/Response~~ Second Preliminary
✓	Check #410.00	____	Issue Fee Transmittal
____	Formal Drawings ___ Sheets	____	Trademark Application and
____	Informal Drawings ___ Sheets		Specimens
____	Assignment w/Form 1595	____	Small Entity Statement
✓	Disclosure Statement w/Form 1449 w/refs	____	Notice to File Missing Parts
✓	Other Second Preliminary Amendment Transmitted		Three 3-Ring Binders

Mailed: Feb. 13, 1998

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
) Group Art Unit: 2785
ELIYAHOU HARARI, ROBERT D.)
NORMAN and SANJAY MEHTROTRA)
)
Serial No.: 08/931,133)
)
Filed: September 18, 1997)
)
For: FLASH EEPROM SYSTEM)
) San Francisco, California

Assistant Commissioner for Patents
Washington, D.C. 20231

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231 on Feb. 13, 1998.

Brenda J. Dolly
Brenda J. Dolly 2/13/98
Signature Date

SECOND PRELIMINARY AMENDMENT TRANSMITTAL

Sir:

Transmitted herewith is a Second Preliminary Amendment in the captioned application.

A check in the amount of $410.00 is enclosed to cover the fee for filing additional claims.

Also enclosed is an Information Disclosure Statement, five sheets of PTO 1449, and three 3-ring binders containing the cited references.

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment,

to Deposit Account No. 13-1030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

Dated: Feb. 11, 1998

Gerald P. Parsons, Reg. No. 24,486
MAJESTIC, PARSONS, SIEBERT & HSUE PC
Four Embarcadero Center, Suite 1100
San Francisco, CA 94111-4106
Telephone: (415) 248-5500
Facsimile: (415) 362-5418

Atty. Docket: HARI.006USG

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

ELIYAHOU HARARI, ROBERT D. NORMAN, and SANJAY MEHROTRA

Serial No.: 08/931,133

Filed: September 16, 1997

For: FLASH EEPROM SYSTEM

Group Art Unit: 2785

San Francisco, California

Hon. Commissioner of
Patents and Trademarks
Washington, D.C. 20231

SECOND PRELIMINARY AMENDMENT

Sir:

Please preliminarily amend the above-identified application, as follows:

IN THE SPECIFICATION:

Page 1, line 1, strike the title and substitute therefor --MULTI-STATE FLASH EEPROM SYSTEM WITH CACHE MEMORY--.

Page 11, line 26, change "Harari" to --Harari, now patent no. 5,095,344,--.

Page 11, lines 28 and 29, strike "filed on the same day as the present application," and substitute the following therefore: --Serial No. 07/337,579, filed April 13, 1989, now abandoned,--.

Page 22, line 14, insert after "204,175" --now patent no. 5,095,344,--.

Page 22, line 16, change "Techniques." to --Techniques, Serial No. 07/337,579, filed April 13, 1989, now abandoned.--

Page 26, line 3, insert a comma --,-- after "204,175" and insert thereafter --now patent no. 5,095,344,--.

Page 26, strike all of line 4, and substitute the following therefore: --Harari, Serial No. 07/337,579, filed April 13, 1989, now abandoned,--.

IN THE CLAIMS:

Add the following new claims:

--68. A method of writing data files into a system of flash EEprom cells that are programmable into more than two states in order to store more than one bit of data per cell, comprising:

temporarily storing, in a cache memory, data files from a host system intended for the flash EEprom memory;

writing data files into the cache memory instead of the flash EEprom memory in response to a write request from the host system;

determining the time since each data file was last written into said cache memory; and

moving from the cache memory a data file having the longest time since last written, when additional space for new data files is required in the cache memory, into the flash EEprom memory by programming individual flash EEPROM cells into one of said more than two programmable states.

69. A method of writing data files into a system of flash EEprom cells that are programmable into more than two states in order to store more than one bit of data per cell, comprising:

temporarily storing, in a cache memory, data files from a host system intended for the flash EEprom memory;

writing data files into the cache memory instead of the flash EEprom memory in response to a write request from the host system;

storing, in a tag memory, the identity of data files and the time each data file was last written into said cache memory; and

by reference to the tag memory, moving a data file having the longest time since last written first from the cache memory to the flash EEprom when additional space for new data files is required in the cache memory, individual flash EEPROM cells being written into one of said more than two programmable states.

70. A method of writing data files into a system of flash EEprom cells that are programmable into more than two states in order to store more than one bit of data per cell, comprising:

temporarily storing, in a cache memory, data files from a host system intended for the flash EEprom memory;

in response to a write request from the host system, writing a data file either into the flash EEprom memory when a previous copy of said data file is not present in the cache memory, or into the cache memory when a previous copy of said data file is present in the cache memory;

moving a data file having the longest time since last written first from the cache memory to the flash EEprom memory when additional space for new data files is required in the cache memory, thereby substantially reducing the number of actual writes to the flash EEprom memory; and

wherein a data file is written into the flash EEPROM by programming individual cells thereof into one of said more than two programmable states.

71. A method of writing data files into a system of flash EEprom cells that are programmable into more than two states in order to store more than one bit of data per cell, comprising:

temporarily storing, in a cache memory, data files from a host system intended for the flash EEprom memory;

in response to a write request from the host system, writing a data file either into the flash EEprom memory when said data file is last written after a predetermined period of time, or into the cache memory when said data file is last written within the predetermined period of time; and

moving from the cache memory a data file having the longest time since last written, when additional space for new data files is required in the cache memory, into the flash EEprom memory by programming individual flash EEPROM cells into one of said more than two programmable states.

72. A method of writing data files into a system of flash EEprom cells that are programmable into more than two states in order to store more than one bit of data per cell, comprising:

temporarily storing, in a cache memory, data files from a host system intended for the flash EEprom memory,

storing, in a tag memory, the identity of data files and the time each data file was last written into said cache memory;

in response to a write request from the host system, writing a data file into the flash EEprom memory when the data file

is not identified in the tag memory, or into the cache memory when the data file is identified in the tag memory;

by reference to the tag memory, moving data file having the longest time since last written first from the cache memory to the flash EEprom memory when additional space for new data files is required in the cache memory; and

wherein a data file is written into the flash EEPROM by programming individual cells thereof into one of said more than two programmable states.--

REMARKS

By this amendment, claims are being added that are directed to the use of cache memory as part of a flash EEPROM system, similar to the existing claims 63-67, but with multi-state operation added. That is, each of the new claims additionally recites that the individual flash EEPROM cells are programmable into more than two states in order to store more than one bit of data per cell.

Although multi-state operation is mentioned in the present application specification, it is more completely discussed in two applications incorporated by reference into the specification at pages 11, 22 and 26. Since the referenced application serial no. 204,175 has issued as patent no. 5,095,344, the patent number is being added by this Amendment. The serial number of the second referenced application is also being added by this Amendment. The status of the second referenced application is that it has become abandoned in favor of a continuation-in-part application which matured into patent no. 5,172,338 and a division thereof into patent no. 5,163,021.

An Information Disclosure Statement is being filed herewith, with copies of the cited references. The 3 patents identified in the preceding paragraph are included.

An early examination and allowance of the present application are solicited.

Respectfully Submitted,

Dated: Feb. 11, 1998

Gerald P. Parsons

Gerald P. Parsons, Reg. No. 24,486
MAJESTIC, PARSONS, SIEBERT & HSUE PC
Four Embarcadero Center, Suite 1100
San Francisco, CA 94111-4106

Docket No.: HARI.006USG

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

ELIYAHOU HARARI, ROBERT D. NORMAN and SANJAY MEHROTRA

Serial No.: 08/931,133

Filed: September 16, 1997

For: FLASH EEPROM SYSTEM

Group Art Unit: 2785

San Francisco, California

Assistant Commissioner of Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

The following Form 1449s (five sheets) and copies of each cited document (three binders) are being filed herewith as an Information Disclosure Statement. Consideration of each of these documents by the Patent Examiner, and the making of each of them of record in the file of this application, is respectfully requested.

Respectfully submitted,

Dated: Feb. 11, 1998.

Gerald P. Parsons

Gerald P. Parsons, Reg. No. 24,486
MAJESTIC, PARSONS, SIEBERT & HSUE PC
Four Embarcadero Center, Suite 1100
San Francisco, CA 94111-4106
Telephone: (415) 248-5500
Facsimile: (415) 362-5418

Atty. Docket: HARI.006USG

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)
) Group Art Unit: 2785
ELIYAHOU HARARI, ROBERT D.)
NORMAN and SANJAY MEHROTRA)
)
Serial No.: 08/931,133)
)
Filed: September 16, 1997)
)
For: FLASH EEPROM SYSTEM)
) San Francisco, California

Assistant Commissioner of Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

The following Form 1449s (five sheets) and copies of each cited document (three binders) are being filed herewith as an Information Disclosure Statement. Consideration of each of these documents by the Patent Examiner, and the making of each of them of record in the file of this application, is respectfully requested.

Respectfully submitted,

Dated: Feb. 11, 1998

Gerald P. Parsons

Gerald P. Parsons, Reg. No. 24,486
MAJESTIC, PARSONS, SIEBERT & HSUE PC
Four Embarcadero Center, Suite 1100
San Francisco, CA 94111-4106
Telephone: (415) 248-5500
Facsimile: (415) 362-5418

Atty. Docket: HARI.006USG

FORM PT01449 (REV. 8-83)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	SERIAL NO.
		HARI.006USG	08/931,133
	INFORMATION DISCLOSURE STATEMENT	APPLICANT	
		Eliyahou Harari et al.	
	(Use several sheets if necessary)	FILED	GROUP
		September 16, 1997	2785

U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	A1	4 0 9 3 9 8 5	1978	Das			
	A2	4 2 7 9 0 2 4	1981	Schrenk			
	A3	4 6 1 6 3 1 1	1986	Sato			
	A4	4 7 1 8 0 4 1	1988	Baglee et al.			
	A5	4 7 8 5 4 2 5	1988	Lavelle			
	A6	4 8 0 0 5 2 0	1989	Iijima			
	A7	4 8 8 7 2 3 4	1989	Iijima			
	A8	4 9 4 9 2 4 0	1990	Iijima			
	A9	5 0 5 3 9 9 0	1991	Kreifels et al.			
	A10	5 0 7 0 4 7 4	1991	Tuma et al.			
	A11	5 0 9 5 3 4 4	1992	Harari			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO
	B1	58 - 2 1 5 7 9 4	1983	Japan			Yes
	B2	58 - 2 1 5 7 9 5	1983	Japan			Yes
	B3	59 - 1 6 2 6 9 5	1984	Japan			Yes
	B4	60 - 2 1 2 9 0 0	1985	Japan			Yes
	B5	62 - 2 8 3 4 9 6	1987	Japan			Yes

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent pages, Etc.)*

	C1	Lucero et al., "A 16 kbit Smart 5 V-only EEPROM with Redundancy," *IEEE Journal of Solid-State Circuits*, vol. SC-18, no. 5, pps. 539-543 (October 1983)
	C2	Torelli et al., "An improved method for programming a word-erasable EEPROM," *Alta Frequenza*, vol. 52, no. 6, pps. 487-494 (Nov.-Dec. 1983)
	C3	Data Sheet: "27F256 256K(32K x 8) CMOS Flash Memory," *Intel Corporation*, pps. 1-24 (May 1988)

EXAMINER	DATE CONSIDERED

*** EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.**

FORM PTO1449 (REV. 8-83)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	SERIAL NO.
		HARI.006USG	08/931,133
	INFORMATION DISCLOSURE STATEMENT	APPLICANT	
		Eliyahou Harari et al.	
	(Use several sheets if necessary)	FILED	GROUP
		September 18, 1997	2785

U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	A12	5 2 2 6 1 6 8	1993	Kobayashi et al.			
	A13	4 2 1 0 9 5 9	1980	Wozniak			
	A14	4 6 4 2 7 5 9	1987	Foster			
	A15	4 4 5 6 9 7 1	1984	Fukuda et al.			
	A16	4 2 9 5 2 0 5	1981	Kunstadt			
	A17	4 6 1 7 6 2 4	1986	Goodman			
	A18	4 3 5 4 2 5 3	1982	Naden			
	A19	4 4 2 2 1 6 1	1983	Kressel et al.			
	A20	4 4 5 0 5 5 9	1984	Bond et al.			
	A21	4 6 5 4 8 4 7	1987	Dutton			
	A22	4 7 3 3 3 9 4	1988	Burkhard			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO
	B6	60 - 0 7 6 0 9 7	1985	Japan			Abstr
	B7	59 - 4 5 6 9 5	1984	Japan			Abstr
	B8	61 - 9 6 5 9 8	1986	Japan			Abstr
	B9	62 - 2 8 3 4 9 7	1987	Japan			Abstr
	B10	63 - 1 8 3 7 0 0	1988	Japan			Abstr

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent pages, Etc.)*

	C4	Preliminary Data Sheet, "48F512 512K Flash EEPROM," *SEEQ Technology, Incorporated*, pps. 2-1 thru 2-12 (October 1988)
	C5	Advanced Data Sheet, "48F010 1024K Flash EEPROM," *SEEQ Technology, Incorporated*, pps. 2-13 thru 2-24 (October 1988)
	C6	Lai, Robert S., *Writing MS-DOS Device Drivers, The Waite Group, Inc.*, September 1987, pp. i-xi and 235-319

EXAMINER	DATE CONSIDERED

*** EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.**

FORM PTO1449 (REV. 8-83)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	SERIAL NO.
		HARI.006USG	08/931.133
	INFORMATION DISCLOSURE STATEMENT	APPLICANT	
		Eliyahou Harari et al.	
	(Use several sheets if necessary)	FILED	GROUP
		September 16, 1997	2785

U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	A23	4 8 9 6 2 6 2	1990	Wayama et al.			
	A24	4 9 4 5 5 3 5	1990	Hosotani et al.			
	A25	4 3 8 0 0 6 6	1983	Spencer et al.			
	A26	4 4 6 3 4 5 0	1984	Haeusele			
	A27	4 3 5 5 3 7 6	1982	Gould			
	A28	3 6 3 3 1 7 5	1972	Harper			
	A29	4 4 9 8 1 4 6	1985	Martinez			
	A30	4 9 2 4 3 3 1	1990	Robinson et al.			
	A31	4 4 7 9 2 1 4	1984	Ryan			
	A32	4 9 5 3 1 2 2	1990	Williams			
	A33	4 9 2 0 5 1 8	1990	Nakamura et al.			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO
	B11	0 0 8 6 8 8 6	1983	European Patent Appln.			
	B12	2 1 3 6 9 9 2 A	1984	UK Patent Appln.			
	B13	0 2 4 3 5 0 3 B1	1987	European Patent Appln.			
	B14	0 3 0 0 2 6 4 B1	1989	European Patent Appln.			
	B15	0 5 5 7 7 2 3	1987	AU Patent Abridgement			

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent pages, Etc.)*

	C7	Miller, "Semidisk Disk Emulator," *Interface Age*, p. 102, November, 1982
	C8	Clewitt, "Bubble Memories as a Floppy Disk Replacement," *1978 MIDCON Technical Papers*, vol. 2, pp. 1-7, Dec. 1978
	C9	Hancock, "Architecting a CCD Replacement for the IBM 2305 Fixed Head Disk Drive," Digest of Papers, *Eighteenth IEEE Computer Society International Conference*, pp. 182-184, 1979
	C10	Wilson, "1-Mbit flash memories seek their role in system design," *Computer Design*, vol. 28, no. 5, pps. 30-32 (March 1989)

EXAMINER	DATE CONSIDERED

*** EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.**

FORM PTO1449 (REV. 8-83)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	SERIAL NO.
		HARI.006USG	08/931,133
	INFORMATION DISCLOSURE STATEMENT	APPLICANT	
	(Use several sheets if necessary)	Eliyahou Harari et al.	
		FILED	GROUP
		September 16, 1997	2785

U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	A34	4 4 9 3 0 7 5	1985	Anderson et al.			
	A35	4 7 9 6 2 3 3	1989	Awaya et al.			
	A36	4 9 1 4 5 2 9	1990	Bonke			
	A37	4 0 5 1 3 5 4	1977	Choate			
	A38	5 1 6 3 0 2 1	1992	Mehrotra et al.			
	A39	4 5 1 4 8 3 0	1985	Hagiwara et al.			
	A40	4 7 9 4 5 6 8	1988	Lim et al.			
	A41	4 6 1 2 6 4 0	1986	Mehrotra et al.			
	A42	4 5 2 7 2 5 1	1985	Nibby, Jr., et al.			
	A43	4 7 4 6 9 9 8	1988	Robinson et al.			
	A44	4 9 4 2 5 5 6	1990	Sasaki et al.			
	A45	4 4 0 5 9 5 2	1983	Slakmon			
	A46	4 6 7 2 2 4 0	1987	Smith et al.			
	A47	4 2 5 0 5 7 0	1981	Tsang et al.			
	A48	4 6 0 1 0 3 1	1986	Walker et al.			
	A49	4 2 8 1 3 9 8	1981	McKenny et al.			
	A50	4 6 1 7 6 5 1	1986	Ip, et al.			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO
	B16	WO 8 4 0 0 6 2 8	1984	PCT W.I.P.O.			
	B17	A0 1 0 5 4 5 4 3	1989	Japanese Patent Abstr.			Yes
	B18	A6 0 1 7 8 5 6 4	1986	Japanese Patent Abstr.			Yes

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent pages, Etc.)*

EXAMINER	DATE CONSIDERED

*** EXAMINER:** Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO1449 (REV. 8-83)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	SERIAL NO.
		HARI.006USG	08/931,133
	INFORMATION DISCLOSURE STATEMENT	APPLICANT	
		Eliyahou Harari et al.	
	(Use several sheets if necessary)	FILED	GROUP
		September 16, 1997	2785

U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	A51	4 4 4 9 2 0 5	1984	Hoffman			
	A52	4 8 0 5 1 0 9	1989	Kroll et al.			
	A53	4 8 2 1 2 4 0	1989	Nakamura et al.			
	A54	4 8 8 2 6 4 2	1989	Tayler et al.			
	A55	4 9 2 0 4 7 8	1990	Furuya et al.			
	A56	4 9 3 3 9 0 6	1990	Terada et al.			
	A57	5 1 3 6 5 4 6	1992	Fukuda et al			
	A58	5 0 5 1 8 8 7	1991	Berger et al.			
	A59	4 9 1 6 6 0 5	1990	Beardsley et al.			
	A60	4 4 6 6 0 5 9	1984	Bastian et al.			
	A61	5 0 4 3 9 4 0	1991	Harari			
	A62	5 1 7 2 3 3 8	1992	Mehrotra et al.			
	A63	5 6 7 1 2 2 9	1997	Harari et al.			
	A64	5 2 9 7 1 4 8	1994	Harari et al.			
	A65	5 3 5 9 5 6 9	1994	Fujita et al.			
	A66	5 4 3 0 8 5 9	1995	Norman et al.			
	A67	5 4 8 8 7 1 1	1996	Hewitt et al.			
	A68	5 6 0 6 5 3 2	1997	Lambrache et al.			
	A69	5 5 4 6 3 5 1	1996	Tanaka et al.			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent pages, Etc.)*

	C11	Bleiker et al., "A Four-State EEPROM Using Floating-Gate Memory Cells," IEEE Journal of Solid-State Circuits, SC-22 (1987) June, No. 3, New York, NY, USA
	C12	Intel Corporation, 27F256, 256K (32K x 8) CMOS FLASH MEMORY, May 1988, pp. 1-21

EXAMINER	DATE CONSIDERED

*** EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.**

FORM PTO1449 (REV. 8-83)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	SERIAL NO.
		HARI.006USG	08/931,133
		APPLICANT	
INFORMATION DISCLOSURE STATEMENT		Eliyahou Harari et al.	
(Use several sheets if necessary)		FILED	GROUP
		September 16, 1997	2785

U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
	A70	5 0 9 5 3 4 4	1992	Harari			
	A71	4 2 7 2 8 3 0	1981	Moench			
	A72	4 2 8 7 5 7 0	1981	Stark			
	A73	4 5 8 6 1 6 3	1986	Koike			
	A74	4 6 5 3 0 2 3	1987	Suzuki et al.			
	A75	4 8 4 7 8 0 8	1989	Kobatake			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO
	C13	Krick, "Three-State MNOS FET Memory Array," IBM Technical Disclosure Bulletin, Vol. 18, No. 12, May 1976, pp. 4192-4193					
	C14	Alberts C.S. et al., "Multi-Bit Storage FET EAROM Cell," IBM Technical Disclosure Bulletin, Vol. 24, No. 74, December 1981, pp 3311-3314					
	C15	Horiguchi et al., "An Experimental Large-Capacity Semiconductor File Memory Using 16-Levels Cell Storage," IEEE Journal of Solid-State Circuits, Vol. 23, No. 1, February 1988, pp.27-33					
	C16	Furuyama, et al., "An Experimental 2-Bit/Cell Storage Dram for Macro Cell or Memory-on-logic Application," 1988 IEEE, pp. 4.4.1 to 4.4.4					
	C17	Stark, "Two Bits Per Cell ROM," 1981 IEEE Catalog No. 81-CH1626-1, pp. 201-212					

EXAMINER	DATE CONSIDERED

*** EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.**